# Pre-Release 2$\mu m$ bRRAM Process

## Support Heterogeneous Integration on Si CMOS Process

INFO SHEET

### GENERAL OVERVIEW

**Technology Features**

- Bulk (area-type) switching, no filaments, 64-level resistive memory technology based on $Al_2O_3/TiO_x$ switching stack.
- Suitable for design acceleration and system integration for embedded memory, near or in memory compute, neuromorphic computing, in sensor compute etc.
- Heterogeneous integration with CMOS
- Low-temperature (350 °C) process
- 4” wafer process capability
- Single cell test chips and arrays (2x2, 3x3, 16x16, 32x32)

**Reliability**

- $SiO_2$ passivated, environmentally stable

**PDKs in AWR and ADS**

- PDK with Virtuoso
- SPICE model, reference designs and library cells

| PARAMETER | UCSD RRAM 2$\mu m$ |
|---|---|
| $V_{set/reset}$ | $\pm$2-3.5 V |
| *Resistance range* | $\pm$10-100MΩ |
| *Pulse width* | $\sim 10\mu s - 100ms$ |
| *Switching* | Area-type |
| *Endurance* | >$10^6$ |
| *Retention* | ~ 2.5y @ 25C |
| *Cell structure* | 1R |
| *Selector* | None |

### FOUNDRY INFORMATION

- UCSD Nanofab
- Full wafer and coupon sized
- Consultation/Design/ /Fab/Testing

**Fab information:**

- https://nanofab.ucsd.edu/

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